AMENDMENTS TO THE SPECIFICATION

Please replace paragraph 3 at page 8, with the following amended paragraph:

Refer now to Fig. 5, schematically depicting the method of the present invention. In this high voltage regulator, the cathode of a diode 38, operating at reverse baize, is connected to a high voltage switch 56. The anode of the diode is connected to one (or more) diode-connected NMOS transistor(s) 40, for example. A diode-connected NMOS transistor is one where the drain and gate are connected. When conducting, the voltage drop across each diode-connected NMOS transistor will be equal to the transistor threshold voltage ~~(V_t)~~ (V).

Please replace the paragraph 4 at page 8, with the following amended paragraph:

Referring still to Fig. 5, the important details of the present invention are illustrated. A plurality (m) of diode connected NMOS transistors 46 are connected in series (i.e. the drain of transistor 40b is connected to the source of transistor 40a, the drain of transistor 46c is connected to the source of transistor 46b, etc.). The source of the diode-connected NMOS transistor(s) 40 is connected to the drain of transistor 46a. The source of the m^{th} transistor 46m is connected to the bias current source 48. The drain of the transistor 62 is connected to the charge pump. The current of transistor 62 will control the pumping frequency of the charge pump. n is the total number of diodes

40 connected in the regulator [[- 40 and 46]]. The diode chain 40 and 46 combined with diode 38 is a high voltage detector circuit. The high voltage detector circuit detects the level of charge pump output. The output of the voltage detector is used to control the pumping frequency of the charge pump.

Please replace the paragraph 3 at page 9, with the following amended paragraph:

The function f the margin erase circuit of the present invention is now described. During normal operation, the bypass switch 50 is opened. The voltage, V_E, generated by the charge pump 36 and regulated by this regulator will be the normal erase voltage (V_{NE}), which is the sum of the voltage drops across the n transistors 46a-46m and 40 and the breakdown voltage (V_{bd}) of the diode 38. Since the voltage drop across each of the transistors ~~transistor~~ 46a-46m and transistors ~~such as~~ 40 (a total of n transistors) is equal to Vt and V, respectively (threshold voltage of NMOS transistor), the normal erase voltage observed at the cathode of the protective diode 38 is given by:

$$V_{NE} = V_{bd} + n*V + m*Vt + V_t\_m1$$

Where V_t_m1 is the threshold voltage of transistor 62. The voltage $V_E = V_{NE}$ is applied to the flash memory 58 through the high voltage switch 56.

Please replace the paragraph 2 at page 10, with the following amended paragraph:

During testing, the bypass switch 50 is closed thereby bypassing transistors 46a-46m. This reduces the voltage observed at the cathode of the diode 38 by $m*V_t$. Thus, the margin erase voltage is given by:

$$V_{ME} = V_{bd} + n*V\ [[-\ m*V_t]] + V_t\_m1$$